A New Field Effect Transistor Which Avoids Pinchoff

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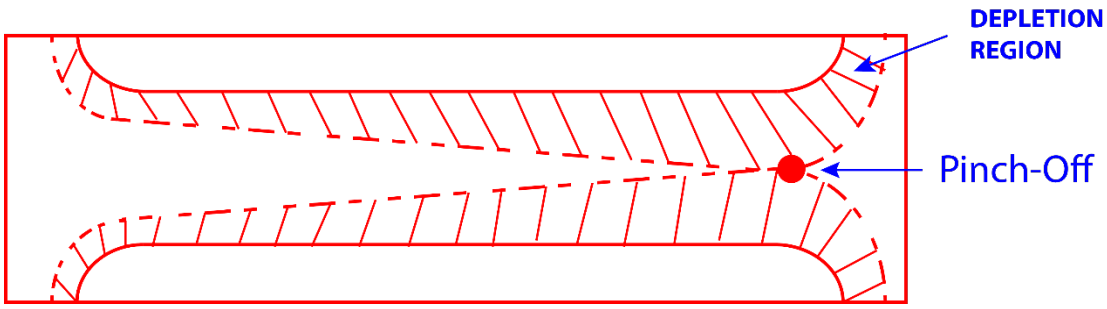
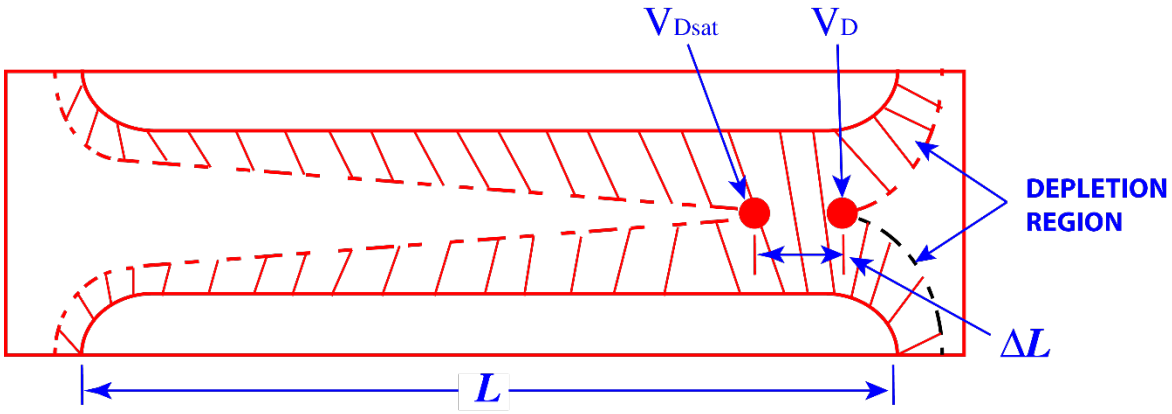
The efficiency of an FET is degraded when the drain voltage is greater than Vdsat; the voltage at which pinchoff first occurs. Under this condition the FET is in saturation where the drain current is not a function of the drain voltage and is only a function of the gate voltage. To understand the degradation of the efficiency let us examine the behavior of an FET in saturation. When the drain voltage of a JFET for instance, is exactly equal to Vdsat, pinchoff occurs exactly at the drain of the transistor as shown in Figure 1(a) [1], If the drain voltage is increased by ΔV, the point at which pinchoff occurs moves towards the source a distance of ΔL, as shown in Figure 1(b). Over the length ΔL, the channel is completely depleted, and the resistance is quite large. Voltage ΔV is dropped across this depleted region and due to the high resistivity in the depleted region, ΔL is very small. For $\Delta L << L$, which represents the usual case, the depletion from source to pinchoff point will be essentially identical in shape and the channel will have essentially the same resistance from the source to the point where pinchoff now occurs. The drain current, which is equal to Vdsat divided by this resistance, hardly changes. This explains why the value of the drain current is nearly constant for drain voltages greater than Vdsat. Over the length ΔL the resistance is quite large, and the power dissipated in this resistance is equal to the product of the saturated current and ΔV. The voltage ΔV does not contribute to the output power and simply degrades the efficiency. It is therefore clear that, for high efficiency pinchoff needs to be avoided and the depletion region must be minimized. Ideally, for converting DC power to RF power, the channel should have no depletion at all for one-half the cycle and should be completely cut-off for the other one-half cycle. With the optimum load, this should yield the maximum DC-to-RF efficiency. To accomplish this, a new (patent pending) FET is proposed, which will be referred to as the "Grayzel FET."



1a.



1b.

Figure 1. The diagrams show the channel of a JFET under different conditions: (a) when the drain voltage equals the pinchoff voltage and (b) when the drain voltage exceeds the pinchoff voltage.

The "Grayzel JFET"

Figure 2 shows a simplified schematic of a JFET with a drain to source DC voltage of seven volts. Points along the channel have values of potential of 0, 1, 2, 3, 4, 5, 6, and 7 V as shown in the figure. The junction is progressively back-biased by these potentials, causing greater depletion at the drain than at the source. Figure 3 shows a simplified schematic diagram of the "Grayzel JFET." The p+ region is divided into N sections that

are insulated from one another, forming N, p-n junctions. (In Figure 3, N is equal to 8 as an illustrative example.) Each p-n junction is biased to ground separately as shown in Figure 3; the first at V_0 and the eighth at $V_0 + 7$. With a drain voltage of seven volts, all of the p-n junctions will have the same DC voltage V_0 across their junctions and hence, to a good approximation the depletion region will be uniform along the channel.

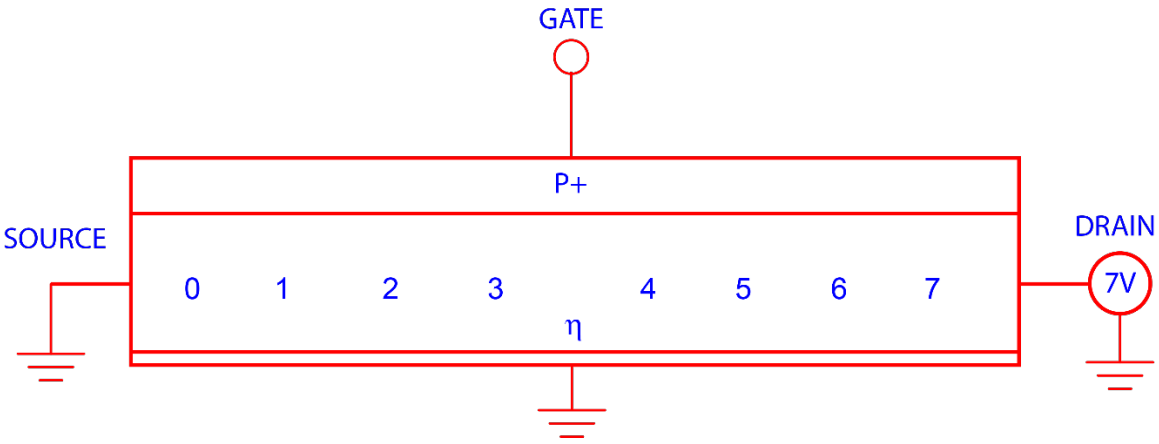


Figure 2. Voltage Drop Down the Channel of a JFET for a Drain Voltage of 7 Volts.

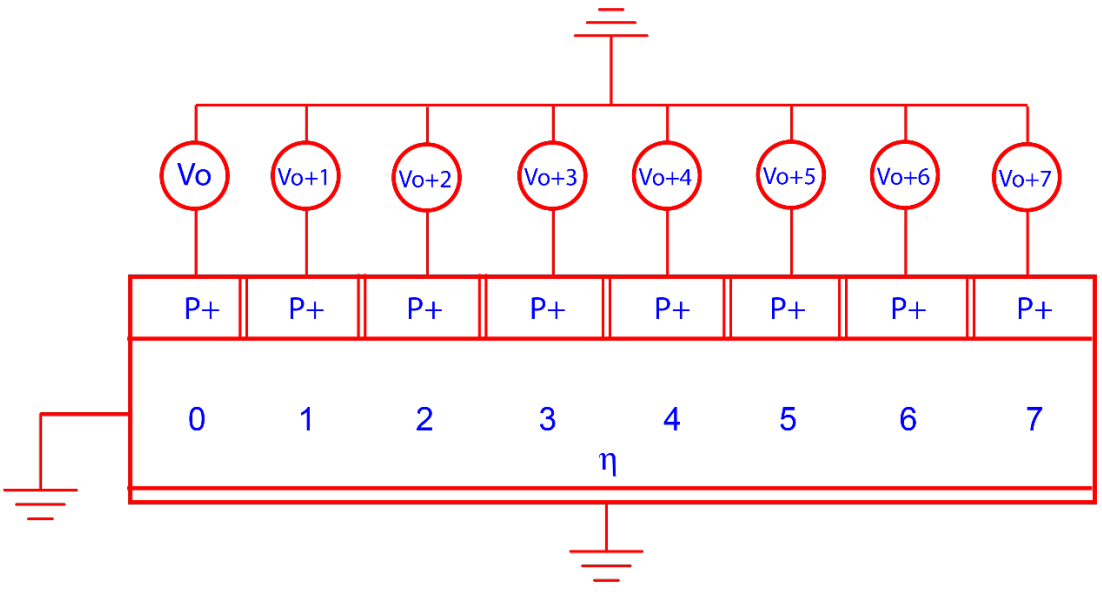


Figure 3. A "Grayzel JFET" where the p-n junctions are individually biased such that each p-n junction is reverse biased at voltage V_0.

Dividing the gate into multiple sections is applicable to all types of FETs. Figure 4 shows an example of the (patent pending) “Grayzel MOSFET” with the gate divided into N sections, with N = 6.

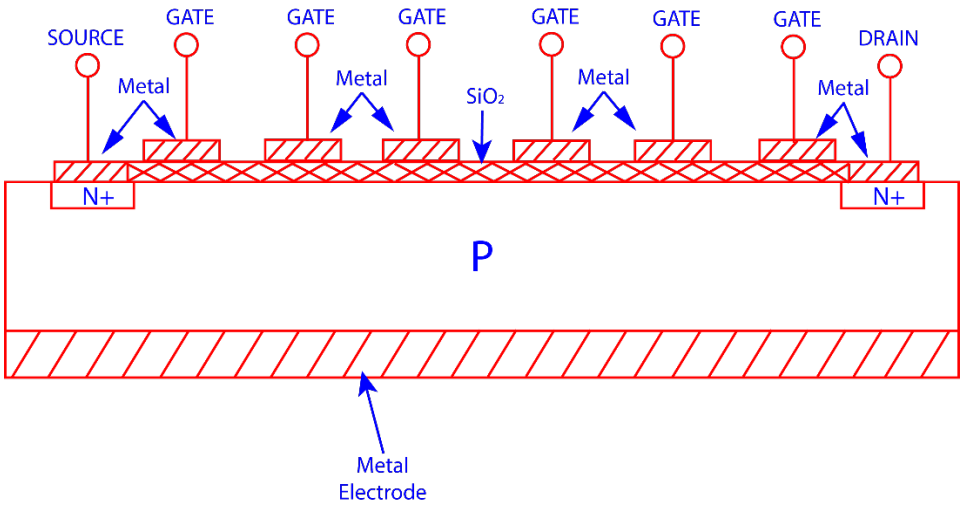


Figure 4. A simplified schematic of a “Grayzel MOSFET”

Figure 5 shows a “Grayzel MOSFET” with a drain voltage of five volts, biased such that each C-MOS capacitor has a voltage of five volts across it. The bias network consists of a ten-volt DC voltage source and six resistors which can be etched onto the chip.

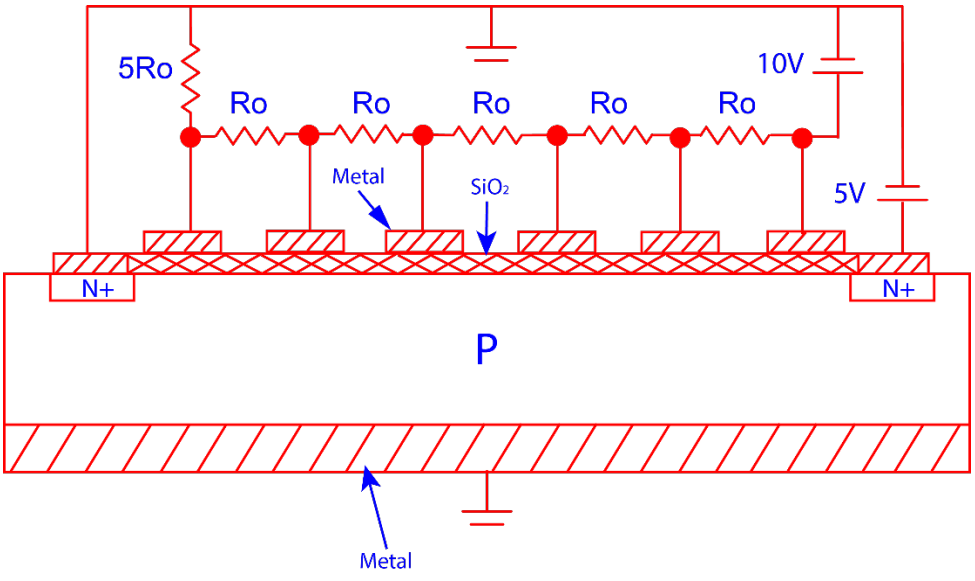


Figure 5. The "Grayzel MOSFET" with a biasing network

Analysis – Special case

We will consider the special case where the odd harmonics are short- circuited and the even harmonics are open-circuited by the load admittance Y(ω) and where for half of the cycle the "Grayzel FET" is cutoff and for the other half of the cycle the depletion region in the channel is of minimal width. The conductance is thus a square wave varying between 0 and G0, where G0 is the conductance when the depletion region in the channel is of minimal width. Let $\theta=2\pi ft=\omega t$, where f is the fundamental frequency of the square wave. The Fourier series of the square wave is given by:

$$G(t) = .5G0 + g(t) \quad (1a)$$

where,

$$g(t) = (2G0/\pi)(\cos\theta - \cos(3\theta)/3 + \cos(5\theta)/5 - \cos(7\theta)/7 + \ldots$$

$$= (2G0/\pi)\sum_{k=1}^{\infty}(-1)^{k-1} \cos[(2k-1)\theta]/ (2k-1) \quad (1b)$$

The FET is terminated in an admittance Y(ω) which at the fundamental frequency has a value G_L. The value of Y(ω) is zero at the even harmonics of the fundamental frequency and infinite at the odd harmonics. The drain voltage therefore, has only even harmonics and the drain current has only odd harmonics.

It is shown in the appendix (Eq. A17), that the output power at the fundamental frequency P1 is given by:

$$P1 = .5(GL)(V_1)^2 = .5G_L[(2/\pi)V_0 /(X+ (2/\pi)^2)]^2 \quad (2)$$

and it is shown in the appendix (Eq. A18) that the efficiency EFF given by:

$$EFF=P1/P0 = (2/\pi)^2 /(X+(2/\pi)^2) \quad (3)$$

Figure 6 shows a plot of the efficiency as a function of X as given by (3).

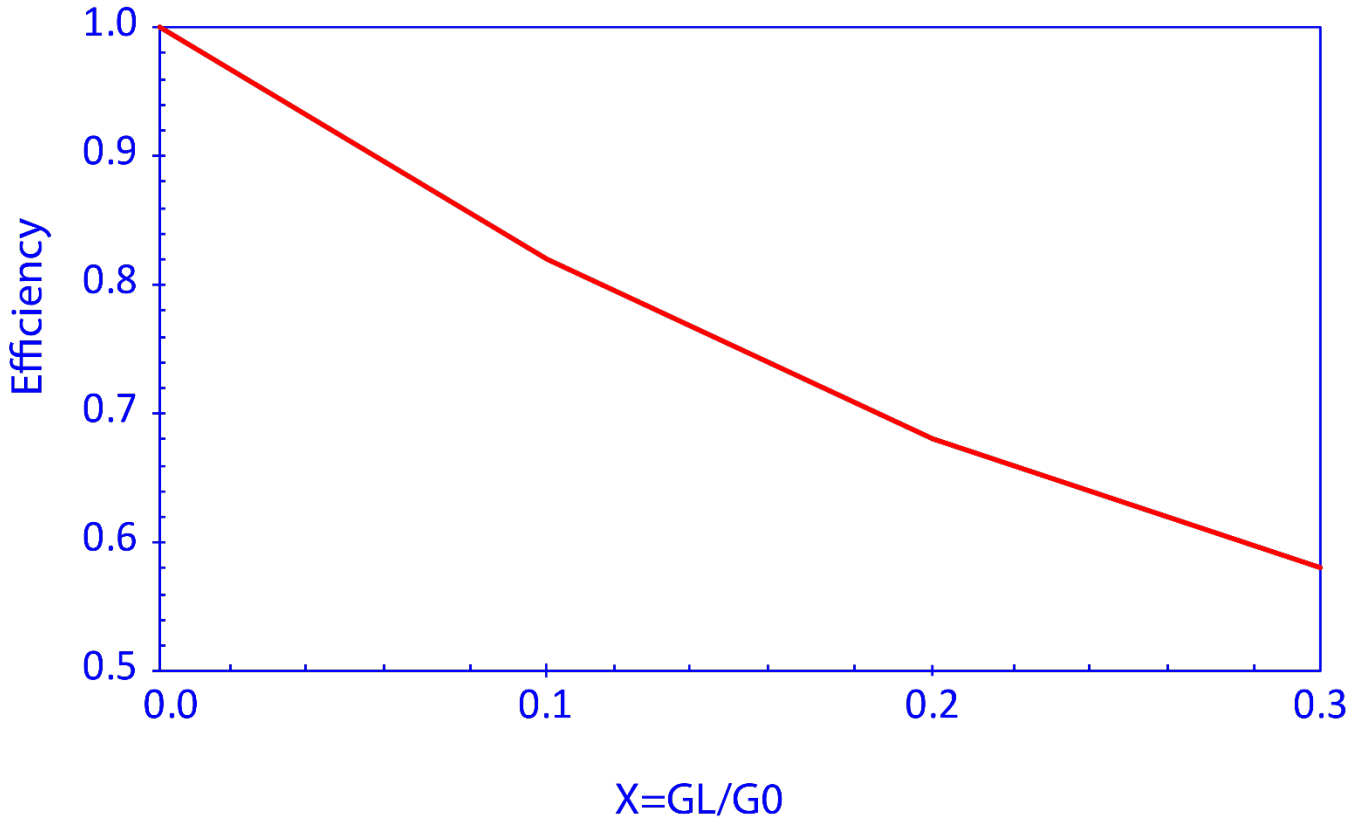


Figure 6. Efficiency as a function of X

This special case where the amplifier is terminated in an open circuit for the even harmonics and a short circuit for the odd harmonics gives good results however, it is not necessarily the optimum termination. An analysis similar to the one performed above, for the special case where the amplifier is terminated in an open circuit for the odd harmonics and a short circuit for the even harmonics gave a poorer result. An optimization needs to be done to determine the optimum termination.

Conclusion:

An FET will have greater efficiency and output power if pinchoff is avoided and the depletion region is made uniform along the channel. Biasing networks have been presented for achieving this condition for an FET whose gate is segmented. The

efficiency and output power have been presented for the case where the odd harmonics are short circuited, and the even harmonics are open circuited and where for half of the cycle the FET is cutoff and for the other half of the cycle the depletion region in the channel is of minimal width**.**

Acknowledgement:

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References:

[1] R. F. Pierret, *Field Effect Devices. Modular Series on Solid State Devices:* Addison-Wesley Publishing Company, 1983, pp. 5-15.

APPENDIX

In this appendix the "Grayzel FET" is analyzed for the case where the odd-order harmonics are short-circuited, and the even-order harmonics are open-circuited and where for half of the cycle the "Grayzel JFET" is cutoff and for half of the cycle there is no depletion in the channel. The conductance G(t) is thus a square wave varying between zero and G_0, where G_0 is the conductance when there is no depletion in the channel. The conductance is given by Eq. A1:

$$G(t) = 0.5G_0 + g(t) \qquad \text{(A1)}$$

Where, g(t) is a square wave of magnitude G0 given by Eq. A2.

$$g(t) = (2G_0/\pi)(\text{Cos}(\theta) - \text{Cos}(3\theta)/3 + \text{Cos}(5\theta)/5 - \text{Cos}(7\theta)/7 + \ldots)$$

$$= (2G0/\pi)\Sigma^{\infty}_{k=1} (-1)^{k-1} \text{Cos}[(2k-1)\theta] /(2k-1) \qquad \text{(A2)}$$

where $\theta = 2\pi ft = \omega t$, and f is the fundamental frequency of the square wave.

The "Grayzel FET" is terminated in an admittance $Y(\omega)$ which at the fundamental frequency is real and has a value $G_L = 1/R_L$. The value of $Y(\omega)$ is zero at the even harmonics and infinite at the odd harmonics of the fundamental frequency. The drain voltage therefore has only even harmonics and the drain current has only odd harmonics. The drain voltage, $V_d(t)$ will have the form of Eq. A3:

$$V_d(t) = V_0 + v(t) \qquad \text{(A3)}$$

where

$$v(t) = V_1 \text{Cos}(\theta) + \Sigma^{\infty}_{k=1} (V_{2k})\text{Cos}(2k\theta) \qquad \text{(A4)}$$

Eq. A4 represents the voltage v(t) for the following reason. The value of the conductance of the channel is equal to G0 when $-90° < \theta < +90°$ and the channel is cutoff during the

remainder of the cycle. Current will therefore only flow when $-90° < \theta < +90°$. Since the current is equal to $V_d(t)G(t)$, $V_d(t)$ will have its maximum value centered at $\theta = 0°$ and will therefore be equal to the sum of cosines.

The bias voltage V_0 in Eq. A3 is the same at all of the segments when the "GRAYZEL FET" is biased as described in this paper. There will however, be a variation of the depletion region along the channel due to v(t). This variation will be small and is neglected in this analysis.

The amplifier shown in Figure A1 where the FET is a "GRAYZEL FET" will be analyzed with the aid of the circuit in Figure A2. Voltage v(t) appears across the RF choke and across the load $Y(\omega)$ which is in series with blocking capacitor C. $V_0+v(t)$ appears across the nonlinear conductance G(t). The choke, which is in series with the DC battery, has voltage v(t) across it but negligible RF current flowing through it. Drain current $I_d(t) = I_0 + i(t)$ is equal to the product $G(t)V_d(t)$. Current i(t) flows in a loop through the termination $Y(\omega)$. DC voltage V_0 appears across the blocking capacitor C.

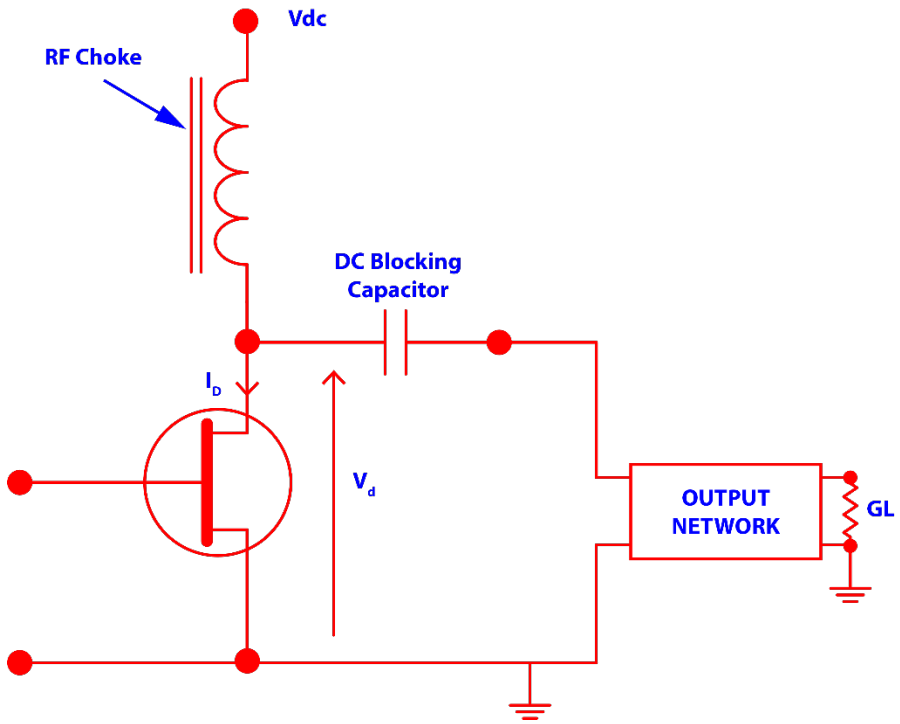

Figure A1. A schematic of a FET amplifier.

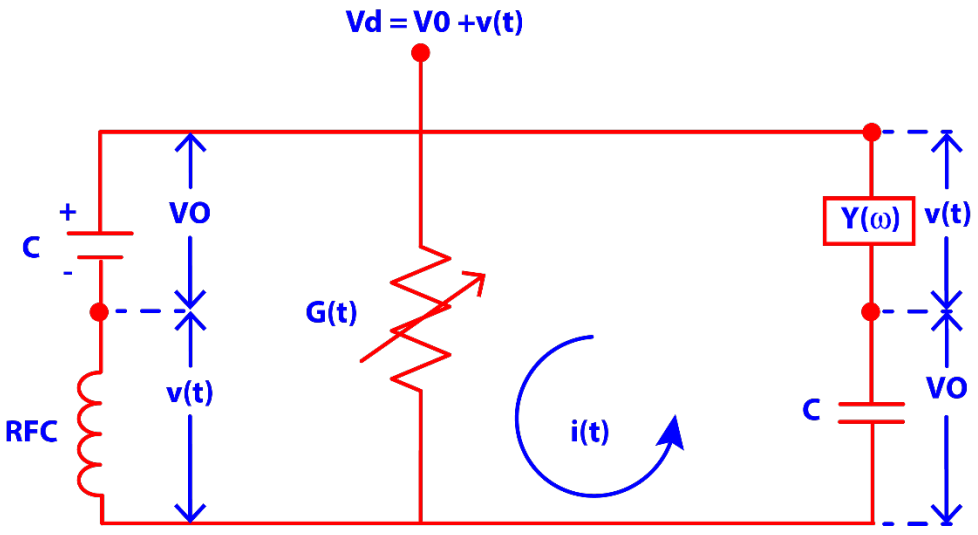

Figure A2. The equivalent circuit of the FET amplifier shown in Figure A1.

The drain current is given by Eq. A5:

$I_d(t) = V_d(t)G(t) = [V_0 + v(t)][0.5G_0 + g(t)]$

$= 0.5V_0G_0 + V_0g(t) + 0.5G_0v(t)+v(t)g(t)$ (A5)

Eqs. A2, A4 and A5 yield for the terms in Eq. A5

$V_0g(t) = (2V_0G_0/\pi)\,(\Sigma^{\infty}_{k=1}(-1)^{k-1}\,\mathrm{Cos}[(2k-1)\theta]\,/[2k-1])$

$0.5G_0v(t) = 0.5G_0\,[\,V_1\,\mathrm{Cos}(\theta) + \Sigma^{\infty}_{k=1}\,V_{2k}\mathrm{Cos}(2k\theta)]$ (A5a)

$v(t)g(t)=(2G_0/\pi)\,[V_1\mathrm{Cos}(\theta)+\Sigma^{\infty}_{k=1}V_{2k}\mathrm{Cos}(2k\theta)]\Sigma^{\infty}_{j=1}(-1)^{j-1}\,\mathrm{Cos}[(2j-1)\theta]\,/(2j-1)$

The drain current can be written as the sum of the DC term, the odd harmonics, and the even harmonics:

$I_d(t) = I_0 + \Sigma^{\infty}_{k=1}(I_{2k-1})\mathrm{Cos}(2k-1)\theta + \Sigma^{\infty}_{k=1}I_{2k}\mathrm{Cos}(2k\theta)$ (A6)

Using the identity $\mathrm{Cos}(x)\mathrm{Cos}(y) = 0.5[\mathrm{Cos}(x + y) + \mathrm{Cos}(x - y)]$, in Eq. A5a the even harmonics can be written as Eq. A7:

$$I_{2k} = G_0[0.5V_{2k} - (2V_1/\pi)(-1)^k / (4k^2 - 1)] \quad \text{(A7)}$$

Since the current at the even harmonics is zero, it is possible to solve for voltage V_{2k} by setting current I_{2k} equal to zero in Eq. A7, yielding Eq. A8:

$$V_{2k} = (4/\pi)(V_1)(-1)^k /(4k^2 - 1) \quad \text{(A8)}$$

Collecting the terms in Cos(θ) in Eq. A5, the value of the current at the fundamental frequency I_1, is given by Eq. A9:

$$I_1 = G_0[2V_0/\pi + 0.5V_1 - (2/\pi) \Sigma^{\infty}_{k=1} (-1)^k V_{2k} / (4k^2-1)] \quad \text{(A9)}$$

Substituting Eq. (A8) into Eq. (A9) yields Eq. (A10):

$$I_1 = G_0 \{2V_0/\pi+V_1 [0.5 - (8/\pi^2) \Sigma^{\infty}_{k=1} 1/ (4k^2-1)^2]\} \quad \text{(A10)}$$

The term $[0.5 - (8/\pi^2) \Sigma^{\infty}_{k=1} 1/ (4k^2-1)^2]$ was found to converge in the limit to $(2/\pi)^2$ as k approaches infinity. (This limit was first estimated and then verified by computer program.) Substituting $(2/\pi)^2$ for $[0.5 - (8/\pi^2) \Sigma^{\infty}_{k=1} 1/ (4k^2-1)^2]$ in Eq. A10 yields Eq. A11

$$I_1 = G_0 [2V_0/ \pi + (2/\pi)^2 V_1] \quad \text{(A11)}$$

At the fundamental frequency $Y(\omega) = G_L$ and $I_1 = - (G_L)(V_1)$. Equating I_1 as given by Eq. A11, to $- (G_L)(V_1)$, yields Eq. A12.

$$2G_0V_0/\pi + G_0V_1(2/\pi)^2 = - G_LV_1 = - XG_0V_1 \quad \text{(A12)}$$

where $X= G_L/G_0 = 1/(G_0R_L)$. Solving Eq. A12 yields Eq. A13:

$$V_1 = - (2/\pi)V_0 / (X+ (2/\pi)^2) \quad \text{(A13)}$$

The DC current I_0 is found from Eq. A5 to have two terms. The first term is $0.5(G_0)(V_0)$ and the second DC term results from the product $(2G_0/\pi)\text{Cos}\theta(V_1\text{Cos}\theta)$. The DC current is given by Eq. A14.

$$I_0 = .5G_0V_0 + G_0V_1/\pi = 0.5G_0V_0[1 + (2/\pi)/(V_1/V_0)] \quad \text{(A14)}$$

Substituting Eq. A13 into Eq. A14 yields:

$$I_0 = 0.5G_0V_0X / (X+(2/\pi)^2) \quad \text{(A15)}$$

The DC power is given by A16:

$$P_0 = I_0V_0 = 0.5G_0V_0^2X / (X+(2/\pi)^2) \quad \text{(A16)}$$

The output power at the fundamental frequency P_1, is found by Eq. A17:

$$P_1 = 0.5G_LV_1^2 = .5G_L[(2/\pi)V_0 /(X+ (2/\pi)^2)]^2 \quad \text{(A17)}$$

The efficiency EFF is then:

$$EFF = P_1/P_0 = (2/\pi)^2 / [X+(2/\pi)^2] \quad \text{(A18)}$$